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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,221	09/30/2003	Rino Micheloni	856063.745	9879

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,221	MICHELONI ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-14* is/are rejected.

7)☒ Claim(s) *7,8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Preliminary Amendment

1. Acknowledgment is made of applicant's Preliminary Amendment, filed 12 December 2003. The changes and remarks disclosed therein were considered.

Claims 1-15 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 30 September 2003. The information disclosed therein was considered.

3. The listing of references in the specification, particularly in the first paragraph, is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

4. Figures 1-3 should be designated by a legend such as --Prior Art-- because it appears that only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header

(as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

In the first paragraph, the reference to a co-pending application should be updated with an application serial number or a patent number, if matured into a patent.

Appropriate correction is required.

6. Claims 4 and 14 are objected to because of the following informalities:

Claim 4 recites "the decode blocks" which appears to lack antecedent basis.

Claim 14 recites "said logic" which appears to lack antecedent basis. It will be understood to depend on claim 13.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 4-6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al. (USPN 5418752) in view of Horiguchi et al. (USPN 5265055) and Horiguchi et al. (USPN 5262993).

Regarding claims 1, 2 and 4, Harari, for example in Figs. 3A and 4 and column 6, lines 26-30 and column 8, lines 23-39, discloses a method for erasing non-volatile memory cells in an integrated non-volatile memory device (Flash EEprom) that comprises a memory cell array organized in a row-and-column layout, and divided in array sectors (Fig. 3A), the method comprising: forcing an incompletely erased sector into a read condition (since erase verification includes a read) whenever the issue of the erase algorithm is incomplete or negative (when an erasure fails due to a defect); scanning the rows of said sector (to identify the failed cell, which would include reading all the rows) to check the possible presence of a spurious current indicating a fail state (due to a short, as one of the recognized defect types; see for example column 7, lines 6-8); identifying and isolating the failed cell (by remapping to a spare cell); re-addressing from said failed cell to a redundant cell within a threshold distance of the failed cell (within the same sector containing the failed cell); and re-starting the erase algorithm (to include the remapped spare cell and to erase verify).

However, Harari does not disclose a row level redundancy (i.e., identifying and isolating a defective row and re-addressing to a spare or redundant row); and at least one switch provided between each one of the decode blocks and respective positive and negative power supplies in order to electrically isolate the failed row.

Horiguchi '055, for example in Fig. 9, discloses an EEPROM (see column 7, line 58) comprising a row level redundancy (with spare word lines SW).

Horiguchi '993, for example in Figs. 1, 4 and 5, discloses an EEPROM (see column 4, line 40) comprising at least one switch (for example, 141 and 142 in Figs. 4 and 5) provided between a memory block (including 20 and 21) and respective power supplies (VPL and VMP associated with the memory block) in order to isolate (or inhibit) a failed block (see for example column 2, lines 61-68). Horiguchi '993 also discloses a short circuit type of failure (resulting in a spurious current) to which the disclosed means is applied (see for example column 2, lines 7-24).

Since a row level redundancy in memories, including EEPROMs, was common and well known in the art (as exemplified by Horiguchi '055), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide redundant rows in each sector of Harari, such that, when an erasure failure is detected, the failed row would be identified and isolated and re-addressed to a redundant row, for the purpose of providing a more space efficient means for repairing multiple defects in different sectors.

Further, since it was common and well known in the art that, in an EEPROM, a positive and a negative voltages are provided to a word line via a word line driver within a row decoder, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the means of Horiguchi '993 to the EEPROM of Horiguchi '055 by providing a switch between the respective negative and positive supplies and the word line driver in order to electrically isolate the failed row, for the purpose of providing a more reliable and robust means for repairing defects of a short circuit type (see for example Horiguchi '993, column 2, lines 7-24 and 44-68), thus increasing the life of such memory.

Regarding claims 5, 6 and 10, the above Harari/Horiguchi/Horiguchi combination further discloses that said re-addressing is effected by means of a redundancy decode block (for example, 600 in Fig. 9 of Horiguchi '055) incorporated inside the row decode circuitry (including 300 in Fig. 9 of Horiguchi '055); that said switches are driven by a logic (including 16 in Fig. 4 of Horiguchi '993) operatively interlinked to the contents of redundancy registers (for example, 35 in Fig. 2 of Horiguchi '993, and 409 in Fig. 5 of Harari); that the redundant row is in the same sector as the sector containing the failed row (for example, 120 within 100 in Fig. 9 of Horiguchi '055).

9. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al. (USPN 5418752) in view of Horiguchi et al. (USPN 5265055) and Horiguchi et al. (USPN 5262993) as applied to claim 1 above, and further in view of Mehrotra et al. (USPN 5659550).

The above Harari/Horiguchi/Horiguchi combination discloses a method as in claim 1, with the exception of checking the possible presence of said spurious discharge current in a conduction path leading to a positive power.

Mehrotra, for example in Figs. 6 and 7, discloses checking the possible presence of a spurious discharge current in a conduction path leading to a positive power (via leakage detector 230 or 240 in Figs. 6 and 7, respectively, of Mehrotra).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the Mehrotra's means for detecting short circuit type defects in the device of the Harari/Horiguchi/Horiguchi combination, for the purpose of easily and reliably identifying such hard defects.

10. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al. (USPN 5418752) in view of Horiguchi et al. (USPN 5265055) and Horiguchi et al. (USPN 5262993) as applied to claim 1 above, and further in view of Shone et al. (USPN 5618742).

The above Harari/Horiguchi/Horiguchi combination discloses a method as in claim 1, with the exception of the redundant row being adjacent the same sector as the sector containing the failed row.

Shone, for example in Fig. 4, discloses a redundant row (within sector 183-1) being adjacent the same sector as the sector containing the failed row (for example, sector 170-N).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of the Harari/Horiguchi/Horiguchi combination, such that the redundant rows are in a separate redundant sector adjacent the sector containing a failed row (as a functionally equivalent alternative arrangement for a row redundancy), for the purpose of sharing the redundant rows among multiple sectors, and reducing the space needed to provide row redundancy for all the sectors.

11. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (USPN 5265055) in view of Horiguchi et al. (USPN 5262993).

Regarding claim 11, Horiguchi '055, for example in Fig. 9, discloses an integrated non-volatile memory device of the programmable and electrically erasable type (EEPROM; see column 7, line 58), comprising a memory cell array organized in a row-and-column layout (within 100-103), and divided in array sectors (100-103), each including at least one row decode

circuit portion (for example, X DEC 300) being supplied positive and negative voltages (inherent in a word line decoder/driver for the EEPROM type), characterized in that it comprises: a redundant row block (120) inside each sector (100); a plurality of row decode blocks (300 and 301) and at least one redundancy decode block (600) within the decode circuitry.

However, Horiguchi '055 does not disclose at least one switch between each one of the decode blocks and the respective positive and negative supplies in order to isolate a failed block during read, program or erase operations.

Horiguchi '993, for example in Figs. 1, 4 and 5, discloses an EEPROM (see column 4, line 40) comprising at least one switch (for example, 141 and 142 in Figs. 4 and 5) between a memory block (20) and respective power supplies (VPL and VMP associated with the memory block) in order to isolate (or inhibit) a failed block during read, program or erase operations (see for example column 2, lines 44-68).

Since it was common and well known in the art that, in an EEPROM, a positive and a negative voltages are provided to a word line via a word line driver within a row decoder, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the means of Horiguchi '993 to the EEPROM of Horiguchi '055 by providing a switch between the respective negative and positive supplies and the word line driver in order to isolate the failed row, for the purpose of providing a more reliable and robust means for repairing defects of a short circuit type (see for example Horiguchi '993, column 2, lines 7-24 and 44-68), thus increasing the life of such memory.

Regarding claims 12-14, the above Horiguchi/Horiguchi combination further discloses that said switches are MOS transistors (141 in Figs. 4 and 5 of Horiguchi '993); a control logic (including 16 in Fig. 4 of Horiguchi '993) for controlling said switches; that the operation of said logic is interlinked with the contents of redundancy registers (for example, 35 in Fig. 2 of Horiguchi '993).

Allowable Subject Matter

12. Claims 7, 8 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 7 and 15, the prior arts of record do not disclose or suggest a method or a device as recited respectively in claim 7 or 15, and particularly, said spurious current is detected by comparison of a row node with a redundancy node, such that the reference signal is produced by a redundant row.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Merchant et al. (USPN 5347489) discloses reference cells for detecting shorted reference cells.

Noda et al. (USPN 5724297) discloses a means to disable a circuit block in a memory.

Smarandoiu et al. (USPN 4538245) discloses a row redundancy in a floating gate memory.

Brennan, Jr. (USPN 5233559) discloses a row redundancy in a flash memory.

Abedifard et al. (USPN 6304488) discloses a flash memory with a switch to a power supply.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

RICHARD ELMS
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